

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(UGC-AUTONOMOUS INSTITUTION)

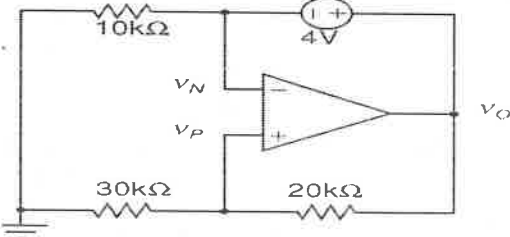
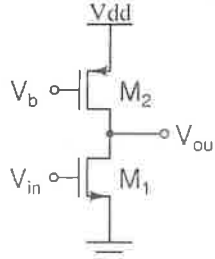
B. Tech III Year II Semester (R23) Regular End Semester Examinations, May – 2026**HONORS: ANALOG IC DESIGN**

(Electronics & Communication Engineering)

Time: 3Hrs**Max Marks: 70**

Attempt all the questions. All parts of the question must be answered in one place only.

All parts of Q.no 1 are compulsory. In Q.no 2 to 6 answer either A or B only

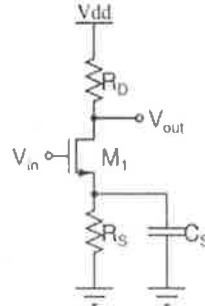
Q. No	Question	Marks	CO	BL
Q.1	i. Define Loop Gain. ii. What is Feedback Factor? iii. Why is a nulling resistor used in series with a Miller capacitor? iv. Which point on the complex plane does the Nyquist plot need to encircle for instability? v. How is Flicker Noise typically modeled in a circuit? vi. How do you reduce the input-referred noise of a CS amplifier? vii. What is the function of an Active Load? viii. What is the "Tail Current" in a differential pair? ix. Specify the primary drawback of the Telescopic Cascode opamp? x. Define Slew Rate.	1M 1M 1M 1M 1M 1M 1M 1M 1M 1M	1 1 2 2 3 3 4 4 5 5	1 1 1 1 1 1 1 1 1 1
Q.2(A)	Derive the closed-loop gain expression for a negative feedback amplifier and discuss the gain-bandwidth trade-off.	12M	1	3
OR				
Q.2(B)	For the circuit shown below, determine V_N , V_P , V_O , the power delivered by the 4V voltage source and power delivered by the opamp.	12M	1	3
				
Q.3(A)	Explain why a phase margin of 60° is often considered ideal in opamp design and how it relates to the system's transient response.	12M	2	2
OR				
Q.3(B)	A negative feedback amplifier has a loop gain $T(s)$ given by the following expression: $T(s) = \frac{1000}{\left(1 + \frac{s}{10^6}\right) \left(1 + \frac{s}{10^7}\right) \left(1 + \frac{s}{10^8}\right)}$ a) Find the Unity Gain Frequency. b) Calculate the Phase Margin of the system. c) Determine if the system is stable.	12M	2	3
Q.4(A)	Derive the expression for the input-referred noise voltage of a common-source amplifier.	12M	3	3
OR				
Q.4(B)	For the circuit shown below, device parameters are as follows. Ignore flicker noise. $V_{dd} = 5V$, $V_{tn} = V_{tp} = 1V$, $\mu_n C_{ox} = 25 \mu A/V^2$; $\lambda_n = \lambda_p = 0.01 V^{-1}$ for $(W/L)_1 = (80\mu m/2\mu m)$; $(W/L)_2 = (40\mu m/2\mu m)$; Bias current = 1mA.	12M	3	3
				
Calculate:				
a) The output resistance of the amplifier.				

- b) The small signal gain of the amplifier.
 c) The input referred thermal noise voltage density of the amplifier.
 d) The total input referred thermal noise voltage in bandwidth of 100MHz bandwidth.

Q.5(A) Analyze the operation of a MOS differential pair with an active load. Derive expressions for the differential gain, common-mode gain, and CMRR. 12M 4 4

OR

Q.5(B) For the circuit shown below, device parameters are as follows. Ignore flicker noise. $V_{dd} = 5V$, $V_{tn} = V_{tp} = 1V$, $\mu_n C_{ox} = 50 \mu A/V^2$, $\mu_p C_{ox} = 25 \mu A/V^2$; $\lambda_n = \lambda_p = 0.01 V^{-1}$ for $(W/L)_1 = (80\mu m/2\mu m)$; Bias current = 0.25 mA; $C_s = 1 pF$; $R_s = 1 k\Omega$; and $R_o = 8 k\Omega$. 12M 4 3

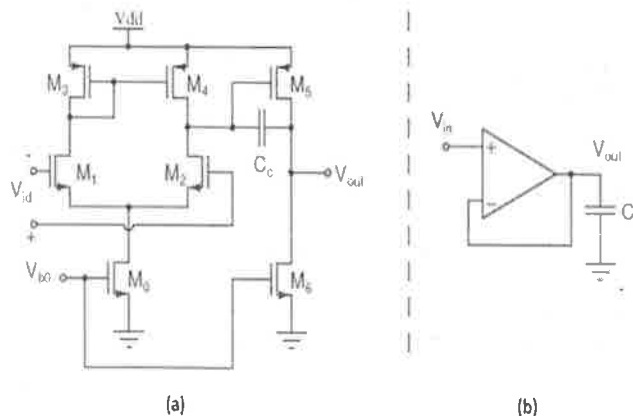


- a) In the expression for the voltage gain of this circuit, determine the value of the pole frequency.
 b) In the expression for the voltage gain of this circuit, determine the value of the zero frequency.
 c) Calculate the magnitude of the small signal voltage gain of the amplifier at very high frequencies.
 d) Calculate the input referred thermal noise voltage density of the amplifier at very high frequencies.

Q.6(A) Describe the architecture of a Telescopic Cascode opamp. Discuss its advantages in terms of gain and speed, and its limitations regarding output swing. 12M 5 2

OR

Q.6(B) For the circuit shown below, device parameters are as follows. Ignore flicker noise. $V_{dd} = 5V$, $V_{tn} = V_{tp} = 1V$, $\mu_n C_{ox} = 50 \mu A/V^2$, $\mu_p C_{ox} = 25 \mu A/V^2$; $\lambda_n = \lambda_p = 0.01 V^{-1}$ for $(W/L)_0 = (128\mu m/2\mu m)$; $(W/L)_{1,2} = (16\mu m/2\mu m)$; $(W/L)_{3,4} = (32\mu m/2\mu m)$; $(W/L)_5 = (320\mu m/2\mu m)$; $(W/L)_6 = (640\mu m/2\mu m)$; $V_{b0} = 1.25V$. The opamp shown in figure (a) below is used in unity gain configuration while driving a load capacitance $C_L = 10 pF$ as shown in figure (b). The opamp is compensated for unity gain configuration Miller Capacitance C_c across gate and drain of M_5 , as shown in figure (a). Neglect all capacitance other than C_c and C_L . 12M 5 3



- a) Determine the low frequency differential mode gain of the opamp of figure (a).
 b) Determine the value of C_c so that the opamp has a phase margin of 60° in unity gain configuration while driving a load capacitance of 10 pF.

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(UGC-AUTONOMOUS INSTITUTION)

B. Tech III Year II Semester (R23) Regular End Semester Examinations, May – 2026**HONORS: DIGITAL IC DESIGN**

(Electronics & Communication Engineering)

Time: 3Hrs**Max Marks: 70**

Attempt all the questions. All parts of the question must be answered in one place only.

All parts of Q.no 1 are compulsory. In Q.no 2 to 6 answer either A or B only

Q. No	Question	Marks	CO	BL
Q.1	i. Define dynamic power dissipation.	1M	1	1
	ii. What is propagation delay?	1M	1	1
	iii. Define fan-out.	1M	2	1
	iv. State the importance of path optimization.	1M	2	1
	v. Define critical path.	1M	3	1
	vi. Draw the circuit diagram of 2 input Domino NAND gate	1M	3	2
	vii. What is hold time?	1M	4	1
	viii. Differentiate between latch and flip flop	1M	4	2
	ix. Write the truth table of full adder	1M	5	2
	x. What is meant by partial product generation	1M	5	2
Q.2(A)	Derive and explain the Voltage Transfer Characteristics (VTC) of CMOS inverter.	12M	1	2
OR				
Q.2(B)	Derive expressions for rise time and fall time in CMOS inverter.	6M	1	2
	Discuss the stacking effect and its role in leakage power reduction.	6M	1	2
Q.3(A)	A logic gate drives a load capacitance of 40 fF through a buffer chain. Determine the optimal number of stages using logical effort approach.	6M	2	3
	Explain logical effort theory with examples.	6M	2	2
OR				
Q.3(B)	Implementation of NAND and NOR gates using CMOS logic.	6M	2	2
	Discuss capacitance effects in combinational logic circuits.	6M	2	3
Q.4(A)	Describe the operation of dynamic CMOS logic circuits.	12M	3	3
OR				
Q.4(B)	A dynamic CMOS gate operates with a clock frequency of 200 MHz and load capacitance of 30 fF. Calculate the dynamic power consumed if $V_{DD} = 1.8$ V.	6M	3	3
	Explain the effect of charge sharing in dynamic logic with suitable numerical example.	6M	3	3
Q.5(A)	Derive the setup and hold time constraints for latch-based timing systems and A latch-based system has clock skew of 1.5 ns, setup time of 2 ns and combinational path delay of 10 ns. Calculate the minimum clock period.	12M	4	4
OR				
Q.5(B)	Explain clock distribution challenges and clock skew reduction techniques in high-speed VLSI systems and Compare latch-based and flip-flop-based timing systems with respect to performance and reliability.	12M	4	4
Q.6(A)	A 4×4 unsigned multiplier multiplies binary numbers 1101 and 1011. Show the complete partial product generation and final addition process.	12M	5	4
OR				
Q.6(B)	Explain carry select adder with suitable diagrams.	12M	5	3

*** END***

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(UGC-AUTONOMOUS INSTITUTION)**B. Tech III Year II Semester (R23) Regular End Semester Examinations, May – 2026****HONORS: VLSI PHYSICAL DESIGN**

(Electronics & Communication Engineering)

Time: 3Hrs**Max Marks: 70**

Attempt all the questions. All parts of the question must be answered in one place only.
All parts of Q.no 1 are compulsory. In Q.no 2 to 6 answer either A or B only

Q.No	Question	Marks	CO	BL
Q.1	i. Define VLSI physical design.	1M	1	1
	ii. What is placement in VLSI?	1M	1	1
	iii. What is routing in VLSI?	1M	2	1
	iv. What is Lee's algorithm?	1M	2	1
	v. Define clock tree synthesis (CTS).	1M	3	1
	vi. What is IR drop?	1M	3	1
	vii. What is DRC?	1M	4	1
	viii. What is ATPG?	1M	4	1
	ix. Define leakage power.	1M	5	1
	x. What is frequency scaling?	1M	5	1
Q.2(A)	Consider a gate array fabrication facility, where the chips designed by three customers X, Y and Z are being fabricated. X orders 5,000 units, Y orders 7,500 units and Z orders 2,500 units of chips. Assume that the cost of fabricating the generic masks corresponding to a design is Rs. 90 lakhs, and the cost of customization is Rs. 15 lakhs for every 500 chips. Calculate the total cost of fabrication of all the 15,000 chips in INR	12M	1	3
OR				
Q.2(B)	Analyze differences between full-custom and standard-cell design styles.	12M	1	4
Q.3(A)	Consider a 25 x 25 grid with the co-ordinates of the lower left and upper right grid cells as (0, 0) and (24, 24) respectively. We are using Hadlock's algorithm to find a path from a source point S to a target point T with co-ordinates (10, 4) and (17, 12) respectively. Calculate the detour number of a cell with co-ordinate (8, 18).	12M	2	3
OR				
Q.3(B)	Compare global vs detailed routing with examples.	12M	2	3
Q.4(A)	Analyze the impact of IR drop on circuit performance.	12M	3	4
OR				
Q.4(B)	A Boolean function is given in Conjunctive Normal Form (CNF) as: $F = (A + B' + C)(A' + C)(B + C')(A + B)$ Convert the given Boolean expression into a format suitable for a SAT solver . Using the DPLL algorithm , determine whether the formula is satisfiable .	12M	3	3
Q.5(A)	Analyze the working of BIST using LFSR and MISR.	12M	4	4

OR

Q.5(B)	Consider an RC tree network shown below: A source drives a network with: $R_1=2\text{ k}\Omega$ connected to node 1 $R_2=3\text{ k}\Omega$ connected from node 1 to node 2 $C_1=1\text{pF}$ at node 1 $C_2=2\text{pF}$ at node 2 Using the Elmore delay model, calculate the delay at node 2. Determine the contribution of each resistor to the total delay. If C_2 is doubled, analyze how the delay changes.	12M	4	3
Q.6(A)	Analyze the impact of Gray coding on switching activity.	12M	5	4
OR				
Q.6(B)	Design a low-power system using multi-level optimization techniques.	12M	5	3
*** END***				